UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,157	12/30/2003	Carlos J. Gonzalez	SNDK.348US0	7914

36257 7590 08/22/2006

PARSONS HSUE & DE RUNTZ LLP
595 MARKET STREET
SUITE 1900
SAN FRANCISCO, CA 94105

EXAMINER	
LI, ZHUO H	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,157	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) *18-27 and 43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 28-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *see action*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I (claims 1-17 and 28-42) in the reply filed on July 26, 2006 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. This application contains claims 18-27 and 43 drawn to an invention nonelected without traverse in reply filed on July 26, 2006. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

3. Accordingly, this Office action is in responds to the reply filed on July 26, 2006, claims 1-17 and 28-42 are pending in the application.

Information Disclosure Statement

4. The Information Disclosure Statements filed on June 21, 2004 and August 5, 2005 have been considered.

Specification

5. The disclosure is objected to because of the following informalities:

A. According to Figure 22, in Paragraph [0080], line 6, --B. Metablock 1 has 2 bad blocks in planes 0* and 1--should be --B. Metablock ~~1~~ [2] has 2 bad blocks in planes 0* and 1--

B. According to Figure 22, in Paragraph [0080], line 7, --C. Metablock 4 has 2 bad blocks in planes 0* and 5--should be -- C. Metablock **4** [3] has 2 bad blocks in planes 0* and 5--

C. According to Figure 22, in Paragraph [0080], line 9, --E. Metablock 7 has 1 bad blocks in planes 0*-- should be -- E. Metablock ~~7~~ [6] has 2 bad blocks in planes 0*--

D. In Paragraph [0080], line 15, --there are no metablocks 2, 3, 6, or 7.--should be there are no metablocks 2, 3, 6, or ~~7~~ [8]-- as defined in Table 1 in paragraph [0081].

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation "said quasi-independent arrays" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 28-34, and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Estakhri et al. (US PAT. 5,835,935 hereinafter Estakhri).

Regarding claim 28, Estakhri discloses a memory system (figure 9) including a controller (200, figure 9) and a non-volatile memory, i.e., mass storage media (212, figure 9), wherein the non-volatile memory is comprises of a plurality of units of erases (102, figure 1 and col. 3 lines 19-32), wherein the controller access the non-volatile memory according to a set of metablock links, i.e., logical block address (LBA0 – LBAN, figure 4), each comprised of a plurality of units of erase, wherein the controller establishes the set of metablock linkings in a deterministic manner (col. 4 lines 32-53).

Regarding claim 29, Estakhri discloses the set of metablock linkings is established according to an algorithm (col. 4 lines 53 through col. 5 line 10).

Regarding claim 30, Estakhri discloses the metablock linkings not formed according to the rule are indicated by a flag (col. 3 line 33 through col. 4 line 15).

Regarding claim 31, Estakhri discloses the flag is maintained in the controller (col. 6 lines 21-49).

Regarding claim 32, Estakhri discloses the flag is maintained in the non-volatile memory (col. 3 line 33 through col. 4 line 15).

Regarding claim 33, Estakhri discloses the algorithm optimizes the set of linkings according to the pattern of defective blocks in the non-volatile memory (figures 4-6 and col. 4 line 55 through col. 5 line 10).

Regarding claim 34, Estakhri discloses the controller determines the pattern of defective blocks in the non-volatile memory based on a scan of the non-volatile memory, i.e., the controller read the records stored in the table to determine the most updated physical address block in the flash memory, wherein the records stored in the table are corresponding to the flag fields (100, figure 1) in the flash memory array (col. 6 lines 21-53).

Regarding claim 36, Estakhri discloses the memory system wherein the set of metablock linkings is updated in response to defects by replacing a defective block in a linking with non-defective block from a list of one or more non-defective blocks, i.e., empty available block, (col. 4 lines 55-67).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 1-17, 35, and 37-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (US PAT. 5,835,935 hereinafter Estakhri) in view of Chien et al. (US PAT. 6,742,078 hereinafter Chien).

Regarding claim 1, Estakhri discloses a method of operating a memory system (figure 9), including a controller (200, figure 9) and a non-volatile memory, i.e., mass storage media (212, figure 9 and col. 6 lines 21-25), wherein the non-volatile memory is comprised of a plurality of units of erase (102, figure 1), the method comprising establishing a set of metablock linkings, i.e., logical block address (LBA0 – LBAN, figure 4), each comprised of a plurality of units of erase, i.e., each one of the clusters stores a sector associated with a single LBA (col. 4 lines 33-53), by which the controller accesses the non-volatile memory (col. 6 lines 34-53), and storing a record i.e., table (144, figure 7 and col. 5 lines 13-51), of the metablock linkings. Estakhri differs from the claimed invention in not specifically teaches a record of the metablock linkings is stored in the non-volatile memory. However, Chien discloses a flash memory system comprising four different types of blocks, data blocks, spare blocks, a new block and a link-table blocks (col. 2 lines 35-53), wherein the link-table blocks comprising a link table which it is used to record the link relationship between the logic block and the actual block (col. 3 lines 51-57 and col. 4 line 55 through col. 5 line 3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the table in the memory

system of Estakhri stores a record of the metablock linkings is in the non-volatile memory, as per teaching by the flash memory system of Chien, because it provides protection against power failure to protect the data link structure and improves stability in use of the flash memory (col. 1 lines 12-15).

Regarding claim 2, Estakhri discloses the record is a completed specification of the set of linkings in terms of units of erase (col. 5 lines 14-51).

Regarding claim 3, Estakhri discloses the set of linkings is formed according to a rule and the record consists of those linkings that are exceptions to the rule (col. 5 line 52 through col. 6 line 20).

Regarding claim 4, Chien discloses the method further comprising determining that a unit of erase in a first of the metablock linkings is defective (col. 3 lines 43-46), updating the first metablock linking so that it no longer contains the defective unit of erase, i.e., stored updated data in a substituted block (col. 3 line 63 through col. 4 line 20), and storing a record of the updated linking in the non-volatile memory (col. 4 lines 10-20).

Regarding claim 5, Chien discloses the method wherein the updating comprises replacing the defective unit of erase with another one of the units of erase, i.e., use a substituted block to stored updated data to replace the defective or original block (col. 3 line 43 through col. 4 line 20).

Regarding claim 6, Chien discloses the method wherein another one of said unit of erase is selected from a list of unlinked units of erase, i.e., spare blocks (col. 3 line 63 through col. 4 line 3).

Regarding claim 7, Chien discloses the method wherein the list of unlinked units of erase is maintained in the non-volatile memory (figure 1 and col. 3 lines 8-30).

Regarding claim 8, Chien discloses the method further comprising subsequent to the replacing the defective unit of erase with another one of the units of erase, i.e., use head and tail pointers to pick the next available spare block in the spare block stack as a substitute block (col. 3 lines 22-41), updating the list of unlinked units of erase (col. 5 lines 18-45).

Regarding claim 9, Chien discloses the method wherein another one of the units of erase is selected from a unit of erase formerly belonging to another linking (col. 4 lines 4-20).

Regarding claim 10, Chien discloses the method further comprising maintaining a list, i.e., spare block stack (figure 4), of unlinked units of erase, determining that one or more units of erase in a first of the metablock linkings is defective, and adding the non-defective units of erase in the first metablock to the list of unlinked units of erase (col. 3 line 65 through col. 4 line 20 and col. 5 lines 18-30).

Regarding claim 11, Chien discloses the method further comprising determining that a unit of erase in a first of the metablock linkings is defective, determining whether an alternate unit of erase is available for the defective unit of erase (col. 3 line 65 through col. 4 line 3), in response to determining that an alternate unit of erase is not available, removing the first metablock from the set of metablock linkings (col. 3 lines 43-46).

Regarding claim 12, Estakhri discloses the non-volatile memory comprises a plurality of quasi-independent arrays, i.e., cluster (116, figure 3), and each of the plurality of units of erase in a given one of the metablock linkings are from a different one of the quasi-independent arrays (col. 4 lines 32-45).

Regarding claim 13, Estakhri discloses the non-volatile memory comprises a plurality of quasi-independent arrays, i.e., cluster (116, figure 3), and the plurality of units of erase (102, figure 3) in a given one of the metablock linkings (col. 4 lines 32-41), the metablock linkings are comprised of pairs of units of erase from the same quasi-independent array, i.e., LBA1 in cluster 1 (figure 3), wherein each of the pairs are from a different one of said quasi-independent arrays, i.e., LBA1 located in cluster 1, LBA2 located in cluster 2 (figure 7 and col. 4 lines 32-67).

Regarding claim 14, Chien discloses a quasi-independent arrays, i.e., flash memories (FM0 – FM3, figure 7) are on separate chips (item a-d, figure 7 and col. 5 lines 31-45).

Regarding claim 15, Chien discloses the method wherein the record of the metablock linkings is stored in a portion of the non-volatile memory other than those assigned for user data (col. 4 line 35 through col. 5 line).

Regarding claim 16, Estakhri discloses each of the units of erase is comprises of plurality of sectors (120, figure 1), and each of the sectors includes a data area (104, figure 1), and an overhead area (110, figure 1), and wherein the record information for those units of erase containing data is maintained in their overhead area (col. 5 lines 13-50).

Regarding claim 17, Chien discloses the method wherein the record information for those units of erase without data is maintained in a portion of the non-volatile memory other than those assigned for user data, i.e., spare block stack (figure 4).

Regarding claim 35, Estakhri differs from the claimed invention in not specifically teaches the memory system comprising the set of metablock linkings is established based on a random allocation. However, Chien discloses a flash memory system comprising four different types of blocks, data blocks, spare blocks, a new block and a link-table blocks (col. 2 lines 35-

53), and both the data blocks, spare blocks, and a link-table blocks are randomly allocate (col. 2 lines 60-67 and col. 5 line 46 through col. 6 line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the set of metablock linkings in the memory system of Estakhri is established based on a random allocation, as per teaching by the flash memory system of Chien, because it saves time to search and write data effectively, and the service life of the flash memory is prolonged (col. 8 lines 1-3).

Regarding claim 37, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 38, Estakhri teaches the memory system wherein the record of the list of one or more non-defective blocks is cached in volatile memory, i.e., RAM (208, figure 9) of the controller (200, figure 9) by said controller (col. 6 lines 21-53).

Regarding claim 39, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 40, the limitations of the claim are rejected as the same reasons set forth in claim 38.

Regarding claims 41-42, Estakhri discloses the memory system wherein an initial set of metablock linkings is established according to an algorithm (col. 5 lines 14-51), and wherein the record of the set of metablock linkings lists only those linkings and units of erase that do not conform to the algorithm (col. 5 line 52 through col. 6 line 20 and col. 6 lines 36-51).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Harari et al. (US PAT. 6,763,480) discloses a flash EEPROM system is capable to remap and replace defective cells with substitute cells, the remapping is performed automatically as soon as a defective cell is detected (col. 1 line 65 through col. 2 line 63).

Garvin et al. (US PAT. 6,260,156) discloses method and system for managing bad areas in flash memory by spare areas, and a working chunk map is created for storing format information and re-mapping information. (abstract).

Wells et al. (US PAT. 5,978,808) discloses virtual small block file manager for flash memory array (abstract).

Unno (US PAT. 6,360,293) discloses solid state disk system having electrically erasable and programmable read only memory (col. 2 lines 5-34).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tues - Fri 9:00am - 6:30pm and alternate Monday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Zhuo H. Li

Patent Examiner
August 18, 2006

SANJIV SHAH
PRIMARY EXAMINER